

## Amba Axi Protocol Specification

This book describes an approach and supporting infrastructure to facilitate debugging the silicon implementation of a System-on-Chip (SOC), allowing its associated product to be introduced into the market more quickly. Readers learn step-by-step the key requirements for debugging a modern, silicon SOC implementation, nine factors that complicate this debugging task, and a new debug approach that addresses these requirements and complicating factors. The authors' novel communication-centric, scan-based, abstraction-based, run/stop-based (CSAR) debug approach is discussed in detail, showing how it helps to meet debug requirements and address the nine, previously identified factors that complicate debugging silicon implementations of SOCs. The authors also derive the debug infrastructure requirements to support debugging of a silicon implementation of an SOC with their CSAR debug approach. This debug infrastructure consists of a generic on-chip debug architecture, a configurable automated design-for-debug flow to be used during the design of an SOC, and customizable off-chip debugger software. Coverage includes an evaluation of the efficiency and effectiveness of the CSAR approach and its supporting infrastructure, using six industrial SOCs and an illustrative, example SOC model. The authors also quantify the hardware cost and design effort to support their approach.

Dynamic and Robust Streaming in and between Connected Consumer-Electronic Devices addresses a subject that is becoming more important over the years. On the one hand the arrival of home networks is imminent, and on the other hand we notice that chips integrate more and more functionality. The home network interconnects the Consumer Electronic (CE) devices in the home, and the individual CE-devices incorporate the chips to realize a ubiquitous streaming of video streams over this network. This book provides a comprehensive overview of the challenges that face us. The book shows that there are many similarities between traditional networking and networks in the chip. However, there are some different operational conditions that lead to original solutions. Dynamic and Robust Streaming in and between Connected Consumer-Electronic Devices focuses on the robustness aspects of the chosen technologies in the area of video streaming. Management of resources such as memory, bandwidth, CPU cycles, bus-cycles is an aspect that is prominent in many of the sections. This book is devoted to recent developments of instrumentation and measurement techniques applied to the aerospace field. It includes 23 selected papers from the 2019 IEEE International Workshop on Metrology for AeroSpace. Measurements are essential for obtaining a deeper knowledge of a phenomenon or an asset, as well as for making proper decisions and proposing new and efficient solutions, and this is especially true in environments as complex as aerospace. The research contributions included in the book can raise the interest of a wide group of researchers, operators and decision-makers from metrology and aerospace fields by presenting the most innovative solutions in this field from the scientific and technological points of view.

The purpose of this book is to evaluate strategies for future system design in multiprocessor system-on-chip (MPSoC) architectures. Both hardware design and integration of new development tools will be discussed. Novel trends in MPSoC design, combined with reconfigurable architectures are a main topic of concern. The main emphasis is on architectures, design-flow, tool-development, applications and system design.

This book constitutes thoroughly refereed post-conference proceedings of the workshops of the 19th International Conference on Parallel Computing, Euro-Par 2013, held in Aachen, Germany in August 2013. The 99 papers presented were carefully reviewed and selected from 145 submissions. The papers include seven workshops that have been co-located with Euro-Par in the previous years: - Big Data Cloud (Second Workshop on Big Data Management in Clouds) - Hetero Par (11th Workshop on Algorithms, Models and Tools for Parallel Computing on Heterogeneous Platforms) - HiBB (Fourth Workshop on High Performance Bioinformatics and Biomedicine) - OMHI (Second Workshop on On-chip Memory Hierarchies and Interconnects) - PROPER (Sixth Workshop on Productivity and Performance) - Resilience (Sixth Workshop on Resiliency in High Performance Computing with Clusters, Clouds, and Grids) - UCHPC (Sixth Workshop on Un Conventional High Performance Computing) as well as six newcomers: - DIHC (First Workshop on Dependability and Interoperability in Heterogeneous Clouds) - Fed ICI (First Workshop on Federative and Interoperable Cloud Infrastructures) - LSDVE (First Workshop on Large Scale Distributed Virtual Environments on Clouds and P2P) - MHPC (Workshop on Middleware for HPC and Big Data Systems) -PADABS (First Workshop on Parallel and Distributed Agent Based Simulations) - ROME (First Workshop on Runtime and Operating Systems for the Many core Era) All these workshops focus on promotion and advancement of all aspects of parallel and distributed computing.

This book describes cutting-edge applications of human factors for sports, injury prevention and outdoor recreation disciplines and provide practical guidance on a range of methods for describing, representing, and evaluating human, team, and system performance in various domains. Contributions in this book show how various human factors methods, applied historically in the complex safety critical domains, are suited to describing and understanding sports performance and sports injury prevention. The book discusses a wealth of methods for different purposes, such as data collection, task analysis (including cognitive task analysis), workload measurement, assessing situation awareness, performance assessment (including team performance assessment), decision making and cognition in sports, human error identification, and interface evaluation methods. With respect to other publications in human factors and ergonomics, which have been more focused on the biomechanical, physiological, environmental, and equipment-related aspects of sports performance, this book gives a special emphasis to research on analysis of individual and team sports, cognitive and social human factors, and covers both sports and outdoor recreation disciplines. Based on the AHFE 2017 Conference on Human Factors in Sports, Injury Prevention and Outdoor Recreation, held on July 17-21, 2017, in Los Angeles, California, USA, this book provides readers with a timely survey of new methods that can be implemented during any sport or outdoor recreation event, and for analyzing and improving the performance and safety of both individuals and teams. Field Programmable Gate Arrays (FPGAs) are currently recognized as the most suitable platform for the implementation of complex digital systems targeting an increasing number of industrial electronics applications. They cover a huge variety of application areas, such as: aerospace, food industry, art, industrial automation, automotive, biomedicine, process control, military, logistics, power electronics, chemistry, sensor networks, robotics, ultrasound, security, and artificial vision. This book first presents the basic architectures of the devices to familiarize the reader with the fundamentals of FPGAs before identifying and discussing new resources that extend the ability of the devices to solve problems in new application domains. Design methodologies are discussed and application examples are included for some of these domains, e.g., mechatronics, robotics, and power systems.

This book constitutes the proceedings of the 21st International Conference on Tools and Algorithms for the Construction and Analysis of Systems, TACAS 2015, which took place in London, UK, in April 2015, as part of the European Joint Conferences on Theory and Practice of Software, ETAPS 2015. The 45 papers included in this volume, consisting of 27 research papers, 2 case-study papers, 7 regular tool papers and 9 tool demonstration papers, were carefully reviewed and selected from 164 submissions. In addition, the book contains one invited contribution. The papers have been organized in topical sections on hybrid systems; program analysis; verification and abstraction; tool demonstrations; stochastic models; SAT and SMT; partial order reduction, bisimulation, and fairness; competition on software verification; parameter synthesis; program synthesis; program and runtime verification; temporal logic and automata and model checking. Verification of real-time requirements in systems-on-chip becomes more complex as more applications are integrated. Predictable and composable systems can manage the increasing complexity using formal verification and simulation. This book explains the concepts of predictability and composability and shows how to apply them to the design and analysis of a memory controller, which is a key component in any real-time system.

The first book to explain the principals behind mobile 3D hardware implementation, helping readers understand advanced algorithms, produce low-cost, low-power SoCs, or become familiar with embedded systems As mobile broadcasting and entertainment applications evolve, there is increasing interest in 3D graphics within the field of mobile electronics, particularly for handheld devices. In Mobile 3D Graphics SoC, Yoo provides a comprehensive understanding of the algorithms of mobile 3D graphics and their real chip implementation methods. 3D graphics SoC (System on a Chip) architecture and its interaction with embedded system software are explained with numerous examples. Yoo divides the book into three sections: general methodology of low power SoC, design of low power 3D graphics SoC, and silicon implementation of 3D graphics SoCs and their application to mobile electronics. Full examples are presented at various levels such as system level design and circuit level optimization along with design technology. Yoo incorporates many real chip examples, including many commercial 3D graphics chips, and provides cross-comparisons of various architectures and their performance. Furthermore, while advanced 3D graphics techniques are well understood and supported by industry standards, this is less true in the emerging mobile applications and games market. This book redresses this imbalance, providing an in-depth look at the new OpenGL ES (The Standard for Embedded Accelerated 3D Graphics), and shows what these new embedded systems graphics libraries can provide for 3D graphics and games developers.

The book covers recent trends in the field of devices, wireless communication and networking. It presents the outcomes of the International Conference in Communication, Devices and Networking (ICCDN 2018), which was organized by the Department of Electronics and Communication Engineering, Sikkim Manipal Institute of Technology, Sikkim, India on 2–3 June, 2018. Gathering cutting-edge research papers prepared by researchers, engineers and industry professionals, it will help young and experienced scientists and developers alike to explore new perspectives, and offer them inspirations on addressing real-world problems in the field of electronics, communication, devices and networking.

This book covers the latest approaches and results from reconfigurable computing architectures employed in the finance domain. So-called field-programmable gate arrays (FPGAs) have already shown to outperform standard CPU- and GPU-based computing architectures by far, saving up to 99% of energy depending on the compute tasks. Renowned authors from financial mathematics, computer architecture and finance business introduce the readers into today's challenges in finance IT, illustrate the most advanced approaches and use cases and present currently known methodologies for integrating FPGAs in finance systems together with latest results. The complete algorithm-to-hardware flow is covered holistically, so this book serves as a hands-on guide for IT managers, researchers and quants/programmers who think about integrating FPGAs into their current IT systems.

This book provides a thorough overview of cutting-edge research on electronics applications relevant to industry, the environment, and society at large. It covers a broad spectrum of application domains, from automotive to space and from health to security, while devoting special attention to the use of embedded devices and sensors for imaging, communication and control. The book is based on the 2019 ApplePies Conference, held in Pisa, Italy in September 2019, which brought together researchers and stakeholders to consider the most significant current trends in the field of applied electronics and to debate visions for the future. Areas addressed by the conference included information communication technology; biotechnology and biomedical imaging; space; secure, clean and efficient energy; the environment; and smart, green and integrated transport. As electronics technology continues to develop apace, constantly meeting previously unthinkable targets, further attention needs to be directed toward the electronics applications and the development of systems that facilitate human activities. This book, written by industrial and academic professionals, represents a valuable contribution in this endeavor.

Communication Architectures for Systems-on-ChipCRC Press

Chip Design and Implementation from a Practical Viewpoint Focusing on chip implementation, Low-Power NoC for High-Performance SoC Design provides practical knowledge and real examples of how to use network on chip (NoC) in the design of system on chip (SoC). It discusses many architectural and theoretical studies on NoCs, including design methodology, topology exploration, quality-of-service guarantee, low-power design, and implementation trials. The Steps to Implement NoC The book covers the full spectrum of the subject, from theory to actual chip design using NoC. Employing the Unified Modeling Language (UML) throughout, it presents complicated concepts, such as models of computation and communication—computation partitioning, in a manner accessible to laypeople. The authors provide guidelines on how to simplify complex networking theory to design a working chip. In addition, they explore the novel NoC techniques and implementations of the Basic On-Chip Network (BONE) project. Examples of real-time decisions, circuit-level design, systems, and chips give the material a real-world context. Low-Power NoC and Its Application to SoC Design Emphasizing the application of NoC to SoC design, this book shows how to build the complicated interconnections on SoC while keeping a low power consumption.

This book constitutes the refereed proceedings of the 24th International Conference on Architecture of Computing Systems, ARCS 2011, held in Lake Como, Italy, in February 2011. The 22 revised full papers presented in seven technical sessions were carefully reviewed and selected from 62 submissions. The papers are organized in topical sections on customization and application specific accelerators; multi/many-core architectures; adaptive system architectures; processor architectures; memory architectures optimization; organic and autonomic computing; network-on-chip architectures.

This book constitutes the refereed proceedings of the 11th International Symposium on Applied Reconfigurable Computing, ARC 2015, held in Bochum, Germany, in April 2015. The 23 full papers and 20 short papers presented in this volume were carefully reviewed and selected from 85 submissions. They are organized in topical headings named: architecture and modeling; tools and compilers; systems and applications; network-on-a-chip; cryptography applications; extended abstracts of posters. In addition, the book contains invited papers on funded R&D - running and completed projects and Horizon 2020 funded projects.

After nearly six years as the field's leading reference, the second edition of this award-winning handbook reemerges with completely updated content and a brand new format. The Computer Engineering Handbook, Second Edition is now offered as a set of two carefully focused books that together encompass all aspects of the field. In addition to complete updates throughout the book to reflect the latest issues in low-power design, embedded processors, and new standards, this edition includes a new section on computer memory and storage as well as several new chapters on such topics as semiconductor memory circuits, stream and wireless processors, and nonvolatile memory technologies and applications.

Details a real-world product that applies a cutting-edge multi-core architecture Increasingly demanding modern applications—such as those used in telecommunications networking and real-time processing of audio, video, and multimedia streams—require multiple processors to achieve computational performance at the rate of a few giga-operations per second. This necessity for speed and manageable power consumption makes it likely that the next generation of embedded processing systems will include hundreds of cores, while being increasingly programmable, blending processors and configurable hardware in a power-efficient manner. Multi-Core Embedded Systems presents a variety of perspectives that elucidate the technical challenges associated with such increased integration of homogeneous (processors) and heterogeneous multiple cores. It offers an analysis that industry engineers and professionals will need to understand the physical details of both software and hardware in embedded architectures, as well as their limitations and potential for future growth. Discusses the available programming models spread across different abstraction levels The book begins with an overview of the evolution of multiprocessor architectures for embedded applications and discusses techniques for autonomous power management of system-level parameters. It addresses the use of existing open-source (and free) tools originating from several application domains—such as traffic

modeling, graph theory, parallel computing and network simulation. In addition, the authors cover other important topics associated with multi-core embedded systems, such as: Architectures and interconnects Embedded design methodologies Mapping of applications

The book provides a comprehensive description and implementation methodology for the Philips/NXP Aethereal/aelite Network-on-Chip (NoC). The presentation offers a systems perspective, starting from the system requirements and deriving and describing the resulting hardware architectures, embedded software, and accompanying design flow. Readers get an in depth view of the interconnect requirements, not centered only on performance and scalability, but also the multi-faceted, application-driven requirements, in particular composability and predictability. The book shows how these qualitative requirements are implemented in a state-of-the-art on-chip interconnect, and presents the realistic, quantitative costs.

This book addresses Software-Defined Radio (SDR) baseband processing from the computer architecture point of view, providing a detailed exploration of different computing platforms by classifying different approaches, highlighting the common features related to SDR requirements and by showing pros and cons of the proposed solutions. It covers architectures exploiting parallelism by extending single-processor environment (such as VLIW, SIMD, TTA approaches), multi-core platforms distributing the computation to either a homogeneous array or a set of specialized heterogeneous processors, and architectures exploiting fine-grained, coarse-grained, or hybrid reconfigurability. Considered a standard industry resource, the Embedded Systems Handbook provided researchers and technicians with the authoritative information needed to launch a wealth of diverse applications, including those in automotive electronics, industrial automated systems, and building automation and control. Now a new resource is required to report on current developments and provide a technical reference for those looking to move the field forward yet again. Divided into two volumes to accommodate this growth, the Embedded Systems Handbook, Second Edition presents a comprehensive view on this area of computer engineering with a currently appropriate emphasis on developments in networking and applications. Those experts directly involved in the creation and evolution of the ideas and technologies presented offer tutorials, research surveys, and technology overviews that explore cutting-edge developments and deployments and identify potential trends. This first self-contained volume of the handbook, Embedded Systems Design and Verification, is divided into three sections. It begins with a brief introduction to embedded systems design and verification. It then provides a comprehensive overview of embedded processors and various aspects of system-on-chip and FPGA, as well as solutions to design challenges. The final section explores power-aware embedded computing, design issues specific to secure embedded systems, and web services for embedded devices. Those interested in taking their work with embedded systems to the network level should complete their study with the second volume: Network Embedded Systems.

New design architectures in computer systems have surpassed industry expectations. Limits, which were once thought of as fundamental, have now been broken. Digital Systems and Applications details these innovations in systems design as well as cutting-edge applications that are emerging to take advantage of the fields increasingly sophisticated capabilities. This book features new chapters on parallelizing iterative heuristics, stream and wireless processors, and lightweight embedded systems. This fundamental text— Provides a clear focus on computer systems, architecture, and applications Takes a top-level view of system organization before moving on to architectural and organizational concepts such as superscalar and vector processor, VLIW architecture, as well as new trends in multithreading and multiprocessing. includes an entire section dedicated to embedded systems and their applications Discusses topics such as digital signal processing applications, circuit implementation aspects, parallel I/O algorithms, and operating systems Concludes with a look at new and future directions in computing Features articles that describe diverse aspects of computer usage and potentials for use Details implementation and performance-enhancing techniques such as branch prediction, register renaming, and virtual memory Includes a section on new directions in computing and their penetration into many new fields and aspects of our daily lives

During the past few years there has been an dramatic upsurge in research and development, implementations of new technologies, and deployments of actual solutions and technologies in the diverse application areas of embedded systems. These areas include automotive electronics, industrial automated systems, and building automation and control. Comprising 48 chapters and the contributions of 74 leading experts from industry and academia, the Embedded Systems Handbook, Second Edition presents a comprehensive view of embedded systems: their design, verification, networking, and applications. The contributors, directly involved in the creation and evolution of the ideas and technologies presented, offer tutorials, research surveys, and technology overviews, exploring new developments, deployments, and trends. To accommodate the tremendous growth in the field, the handbook is now divided into two volumes. New in This Edition: Processors for embedded systems Processor-centric architecture description languages Networked embedded systems in the automotive and industrial automation fields Wireless embedded systems Embedded Systems Design and Verification Volume I of the handbook is divided into three sections. It begins with a brief introduction to embedded systems design and verification. The book then provides a comprehensive overview of embedded processors and various aspects of system-on-chip and FPGA, as well as solutions to design challenges. The final section explores power-aware embedded computing, design issues specific to secure embedded systems, and web services for embedded devices. Networked Embedded Systems Volume II focuses on selected application areas of networked embedded systems. It covers automotive field, industrial automation, building automation, and wireless sensor networks. This volume highlights implementations in fast-evolving areas which have not received proper coverage in other publications. Reflecting the unique functional requirements of different application areas, the contributors discuss inter-node communication aspects in the context of specific applications of networked embedded systems.

System-on-Chip (SoC) represents the next major market for microelectronics, and there is considerable interest world-wide in developing effective methods and tools to support the SoC paradigm. SoC is an expanding field, at present the technical and technological literature about the overall state-of-the-art in SoC is dispersed across a wide spectrum which includes books, journals, and conference proceedings. The book provides a comprehensive and accessible source of state-of-the-art information on existing and emerging SoC key research areas, provided by leading experts in the field. This book covers the general principles of designing, validating and testing complex embedded computing systems and their underlying tradeoffs. The book has twenty five chapters organised into eight parts, each part focuses on a particular topic of SoC. Each chapter has some background covering the basic principles, and extensive list of references. It is aimed at graduate students, designers and managers working in Electronic and Computer engineering.

"This book has collected the latest research within the field of real-time systems engineering, and will serve as a vital reference compendium for practitioners and academics"--Provided by publisher.

This book covers key concepts in the design of 2D and 3D Network-on-Chip interconnect. It highlights design challenges and discusses fundamentals of NoC technology, including architectures, algorithms and tools. Coverage focuses on topology exploration for both 2D and 3D NoCs, routing algorithms, NoC router design, NoC-based system integration, verification and testing, and NoC reliability. Case studies are used to illuminate new design methodologies.

This book discusses the design and performance analysis of SDRAM controllers that cater to both real-time and best-effort applications, i.e. mixed-time-criticality memory controllers. The authors describe the state of the art, and then focus on an architecture template for reconfigurable memory controllers that addresses effectively the quickly evolving set of

SDRAM standards, in terms of worst-case timing and power analysis, as well as implementation. A prototype implementation of the controller in SystemC and synthesizable VHDL for an FPGA development board are used as a proof of concept of the architecture template.

This book constitutes the proceedings of the International Joint Conference on Rules and Reasoning, RuleML+RR 2019, held in Bolzano, Italy, during September 2019. This is the third conference of a new series, joining the efforts of two existing conference series, namely “RuleML” (International Web Rule Symposium) and “RR” (Web Reasoning and Rule Systems). The 10 full research papers presented together with 5 short technical communications papers were carefully reviewed and selected from 26 submissions.

This book constitutes the refereed proceedings of the 12th International Symposium on Applied Reconfigurable Computing, ARC 2016, held in Rio de Janeiro, Brazil, in March 2016. The 20 full papers presented in this volume were carefully reviewed and selected from 47 submissions. They are organized in topical headings named: video and image processing; fault-tolerant systems; tools and architectures; signal processing; and multicore systems. In addition, the book contains 3 invited papers and 8 poster papers on funded RD running and completed projects.

In Interconnect-centric Design for Advanced SoC and NoC, we have tried to create a comprehensive understanding about on-chip interconnect characteristics, design methodologies, layered views on different abstraction levels and finally about applying the interconnect-centric design in system-on-chip design. Traditionally, on-chip communication design has been done using rather ad-hoc and informal approaches that fail to meet some of the challenges posed by next-generation SOC designs, such as performance and throughput, power and energy, reliability, predictability, synchronization, and management of concurrency. To address these challenges, it is critical to take a global view of the communication problem, and decompose it along lines that make it more tractable. We believe that a layered approach similar to that defined by the communication networks community should also be used for on-chip communication design. The design issues are handled on physical and circuit layer, logic and architecture layer, and from system design methodology and tools point of view. Formal communication modeling and refinement is used to bridge the communication layers, and network-centric modeling of multiprocessor on-chip networks and socket-based design will serve the development of platforms for SoC and NoC integration. Interconnect-centric Design for Advanced SoC and NoC is concluded by two application examples: interconnect and memory organization in SoCs for advanced set-top boxes and TV, and a case study in NoC platform design for more generic applications.

Two large international conferences on Advances in Engineering Sciences were held in Hong Kong, March 18–20, 2015, under the International MultiConference of Engineers and Computer Scientists (IMECS 2015), and in London, UK, 1–3 July, 2015, under the World Congress on Engineering (WCE 2015) respectively. This volume contains 35 revised and extended research articles written by prominent researchers participating in the conferences. Topics covered include engineering mathematics, computer science, electrical engineering, manufacturing engineering, industrial engineering, and industrial applications. The book offers state-of-the-art advances in engineering sciences and also serves as an excellent reference work for researchers and graduate students working with/on engineering sciences.

This book provides a unified overview of network-on-chip router micro-architecture, the corresponding design opportunities and challenges, and existing solutions to overcome these challenges. The discussion focuses on the heart of a NoC, the NoC router, and how it interacts with the rest of the system. Coverage includes both basic and advanced design techniques that cover the entire router design space including router organization, flow control, pipelined operation, buffering architectures, as well as allocators' structure and algorithms. Router micro-architectural options are presented in a step-by-step manner beginning from the basic design principles. Even highly sophisticated design alternatives are categorized and broken down to simpler pieces that can be understood easily and analyzed. This book is an invaluable reference for system, architecture, circuit, and EDA researchers and developers, who are interested in understanding the overall picture of NoC routers' architecture, the associated design challenges, and the available solutions.

Platform Based Design at the Electronic System Level presents a multi-faceted view of the challenges facing the electronic industry in the development and integration of complex heterogeneous systems, including both hardware and software components. It analyses and proposes solutions related to the provision of integration platforms by System on Chip and Integrated Platform providers in light of the needs and requirements expressed by the system companies: they are the users of such platforms, which they apply to develop their next-generation products. This is the first book to examine ESL from perspectives of system developer, platform provider and Electronic Design Automation.

This book constitutes the refereed proceedings of the 23st International Symposium on VLSI Design and Test, VDAT 2019, held in Indore, India, in July 2019. The 63 full papers were carefully reviewed and selected from 199 submissions. The papers are organized in topical sections named: analog and mixed signal design; computing architecture and security; hardware design and optimization; low power VLSI and memory design; device modelling; and hardware implementation.

This book constitutes the thoroughly refereed conference proceedings of the 18th International Workshop on Formal Methods for Industrial Critical Systems, FMICS 2013, held in Madrid, Spain, in September 2013. The 13 papers presented were carefully selected from 25 submissions and cover topics such as design, specification, code generation and testing based on formal methods, methods, techniques and tools to support automated analysis, certification, debugging, learning, optimization and transformation of complex, distributed, dependable, real-time systems and embedded systems, verification and validation methods, tools for the development of formal design descriptions, case studies and experience reports on industrial applications of formal methods, impact of the adoption of formal methods on the development process and associated costs, application of formal methods in standardization and industrial forums.

We are delighted to welcome readers to the proceedings of the 6th Pacific-Rim Conference on Multimedia (PCM). The first PCM was held in Sydney, Australia, in 2000. Since then, it has been hosted successfully by Beijing, China, in 2001, Hsinchu, Taiwan, in 2002, Singapore in 2003, and Tokyo, Japan, in 2004, and finally Jeju, one of the most beautiful and fantastic islands in Korea. This year, we accepted 181 papers out of 570 submissions including regular and special session papers. The acceptance rate of 32%

indicates our commitment to ensuring a very high-quality conference. This would not be possible without the full support of the excellent Technical Committee and anonymous reviewers that provided timely and insightful reviews. We would therefore like to thank the Program Committee and all reviewers. The program of this year reflects the current interests of the PCM's. The accepted papers cover a range of topics, including, all aspects of multimedia, both technical and artistic perspectives and both theoretical and practical issues. The PCM 2005 program covers tutorial sessions and plenary lectures as well as regular presentations in three tracks of oral sessions and a poster session in a single track. We have tried to expand the scope of PCM to the artistic papers which need not to be strictly technical.

This book provides an overview of current Intellectual Property (IP) based System-on-Chip (SoC) design methodology and highlights how security of IP can be compromised at various stages in the overall SoC design-fabrication-deployment cycle. Readers will gain a comprehensive understanding of the security vulnerabilities of different types of IPs. This book would enable readers to overcome these vulnerabilities through an efficient combination of proactive countermeasures and design-for-security solutions, as well as a wide variety of IP security and trust assessment and validation techniques. This book serves as a single-source of reference for system designers and practitioners for designing secure, reliable and trustworthy SoCs.

The ARCS series of conferences has over 30 years of tradition reporting top-notch results in computer architecture and operating systems research. It is organized by the special interest group on "Computer and System Architecture" of the GI (Gesellschaft für Informatik e.V.) and ITG (Informationstechnische Gesellschaft im VDE - Information Technology Society). In 2009, ARCS was hosted by the Delft University of Technology, which has one of the leading information technology schools in Europe. This year's special focus was set on energy awareness viewed from two different perspectives. Firstly, this deals with the improvement of computer systems to be as energy-efficient as possible (particularly for specific applications). One can think of heterogeneous multi-core architectures or reconfigurable architectures for this purpose. Secondly, this addresses the usage of computer systems to reduce the energy consumption of other systems, which might lead to problems of communication and cooperation. Like the previous conferences in this series, it continues to be an important forum for computer architecture research. The call for papers resulted in a total of 57 submissions from around the world. Each submission was assigned to at least three members of the Program Committee for review. The Program Committee decided to accept 21 papers, which are arranged into eight sessions. The accepted papers are from: Finland, France, Germany, Japan, The Netherlands, Singapore, Spain, UK, and USA. Three intriguing keynotes from academia and industry complemented the strong technical program.

A presentation of state-of-the-art approaches from an industrial applications perspective, Communication Architectures for Systems-on-Chip shows professionals, researchers, and students how to attack the problem of data communication in the manufacture of SoC architectures. With its lucid illustration of current trends and research improving the performance, quality, and reliability of transactions, this is an essential reference for anyone dealing with communication mechanisms for embedded systems, systems-on-chip, and multiprocessor architectures—or trying to overcome existing limitations. Exploring architectures currently implemented in manufactured SoCs—and those being proposed—this book analyzes a wide range of applications, including: Well-established communication buses Less common networks-on-chip Modern technologies that include the use of carbon nanotubes (CNTs) Optical links used to speed up data transfer and boost both security and quality of service (QoS) The book's contributors pay special attention to newer problems, including how to protect transactions of critical on-chip information (personal data, security keys, etc.) from an external attack. They examine mechanisms, revise communication protocols involved, and analyze overall impact on system performance.

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